NLB1 Series LPDDR2 SDRAM – 1Gb (x32)

Overview

The 1Gb Mobile Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 1,073,741,824 bits. The LPDDR2-S4 device is internally configured as an eight-bank DRAM. Each of the x32's 134,217,728-bit banks is organized as 8,192 rows by 512 columns by 32 bits.

Mobile LPDDR2 is a high-speed SDRAM internally configured as a 8-bank memory device. LPDDR2 devices use a double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system.

The 10-bit CA bus is used to transmit command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the rising and falling edges of the clock.

LPDDR2-S4 devices use a double data rate architecture on the DQ pins to achieve high-speed operation. The double data rate architecture is essentially a 4n pre-fetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or WRITE access for the LPDDR2-S4 effectively consists of a single 4n-bit-wide, one-clock-cycle data transfer at

the internal SDRAM core and four corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an ACTIVATE command followed by a READ or WRITE command. The address and BA bits registered coincident with the ACTIVATE command are used to select the row and bank to be accessed.

The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

Features

- Functionality
  - VDD2 = 1.14–1.30V
  - VDDCA/VDDQ = 1.14–1.30V
  - VDD1 = 1.70–1.95V
  - Interface: HSUL_12
  - Data width: x32
  - Clock frequency range: 400 - 10MHz
  - Four-bit pre-fetch DDR architecture
  - Eight internal banks for concurrent operation
  - Multiplexed, double data rate, command/address inputs; commands entered on every CK edge
  - Bidirectional/differential data strobe per byte of data (DQS/DQS#).
  - DM masks write date at the both rising and falling edge of the data strobe
  - Programmable READ and WRITE latencies (RL/WL)
  - Programmable burst lengths: 4, 8, or 16
  - Auto refresh and self refresh supported
  - All bank auto refresh and per bank auto refresh supported
  - Clock stop capability
- Configuration
  - 32M X 32 (4M X 32 X 8Banks)
- Low Power Features
  - Low voltage power supply.
  - Auto TCSR (Temperature Compensated Self Refresh).
  - PASR (Partial Array Self Refresh) power-saving mode.
  - DPD (Deep Power Down) Mode.
  - DS (Driver Strength) Control.
- Operating temperature range:
  - Extended Test (ET): -25~85°C
  - Industrial (IT): -40~85°C
- Timing – Cycle Time
  - 2.5ns @ RL = 6
  - 3.0ns @ RL = 5
- Package
  - 134-ball FBGA (10.0mm x 11.5mm x 1.0mm)
- Addressing
  - Number of banks: 8
  - Bank address: BA [2:0]
  - Row: R [12:0]
  - Column[1]: C [8:0]

Note: The least-significant column address CA0 is not transmitted on the CA bus, and is implied to be zero.

How to Order

Function	Density	IO Width	Pkg Type	Pkg Size	Speed & Latency	Option	INSIGNIS PART NUMBER:
LPDDR2	1Gb	X32	FBGA	10x11.5(x1.0)	DDR400	Extended Test	NLB13PFL-2AET
LPDDR2	1Gb	X32	FBGA	10x11.5(x1.0)	DDR400	Industrial Temp	NLB13PFL-2AIT

** Engineering Specifications are available upon request by emailing info@insignis-tech.com*