NLD5 Series LPDDR SDRAM – 512Mb (x32)

Overview

The 512Mb Low Power DDR SDRAM is a high-speed CMOS, dynamic random-access memory (DRAM) organized as 16M x 32 and containing 536,870,912 bits. It is internally configured as a quad-bank DRAM. Each of the 134,217,728-bits banks is organized as 8,192 rows by 512 columns by 32 bits. These devices feature advanced circuit design to provide low active current and extremely low standby current. The device is compatible with the JEDEC standard Low Power DDR SDRAM specifications.

The 512Mb Low Power DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n-prefetch architecture with an interface designed to transfer four data words per clock cycle at the I/O balls. A single read or write access for the 512Mb DDR SDRAM effectively consists of a single 2n-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the Low Power DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The X32 offering has two data strobes.

The 512Mb Low Power DDR SDRAM operates from a differential clock (CLK and /CLK); the crossing of CLK going HIGH and /CLK going LOW will be referred to as the positive edge of CLK. Commands (address and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CLK.

Read and write accesses to the Low Power DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access. The DLL signal that is typically used on standard DDR devices is not necessary on the Low Power DDR SDRAM. It has been omitted to save power.

The Low Power DDR SDRAM provides for programmable READ or WRITE burst lengths of 2,4,8 or 16. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of Low Power DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto-refresh mode is provided, along with a power saving power-down mode. Self refresh mode offers temperature compensation through an on-chip temperature sensor and partial array self refresh, which allow users to achieve additional power saving. The temperature sensor is enabled by default and the partial array self refresh can be programmed through the extended mode register.

Features

- Functionality
  - Double-data-rate architecture; two data transfers per CLK cycle.
  - Bidirectional data strobe per byte data (DQS).
  - No DLL; CLK to DQS is not Synchronized.
  - Differential CLK inputs (CLK and /CLK).
  - Commands entered on each positive CLK edge.
  - DQS edge-aligned with data for Reads; center-aligned with data for Writes.
  - Four internal banks for concurrent operation.
  - Data masks (DM) for masking write data-one mask per byte.
  - Programmable burst lengths: 2, 4, 8, 16.
  - Programmable CAS Latency: 2, 3.
  - Concurrent auto pre-charge option is supported.
  - Auto refresh and self refresh modes.
  - Status read register (SRR)
  - LVCMOS-compatible inputs.
- Configuration
  - 16M X 32 (4M X 32 X 4Banks)
- Low Power Features
  - Low voltage power supply.
  - Auto TCSR (Temperature Compensated Self Refresh).
  - Partial Array Self Refresh power-saving mode.
  - Deep Power Down Mode.
  - Driver Strength Control.
- Operating temperature range:
  - Extended Test (ET): -25~85°C
  - Industrial (IT): -40~85°C
- Package
  - 90-Ball FBGA (8 X 13 X 0.8mm)

How to Order

Function	Density	IO Width	Pkg Type	Pkg Size	Speed & Latency	Option	INSIGNIS PART NUMBER:
LPDDR	512Mb	X32	FBGA	8x13(x1.0)	PC166	Extended Test	NLD53PFJ-16ET
LPDDR	512Mb	X32	FBGA	8x13(x1.0)	PC166	Industrial Temp	NLD53PFJ-16IT
LPDDR	512Mb	X32	FBGA	8x13(x1.0)	PC200	Extended Test	NLD53PFJ-20ET
LPDDR	512Mb	X32	FBGA	8x13(x1.0)	PC200	Industrial Temp	NLD53PFJ-20IT

** Engineering Specifications are available upon request by emailing* ***info@insignis-tech.com***